Fermilab

Particle Physics/Electrical Engineering Department

Specification for Production
CMS QIE ASIC
(QIE8)

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9/27/02

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Revision History

Date	Name	
2/2/01	TMS	Added timing information for RESET
8/28/02	TMS	Production pinout information added
9/27/02	TMS	General editing

CMS QIE (QIE8) Overview

The QIE8 is the latest addition to the "family" of QIE devices. It is the first of a new generation of parts which contain major design changes and improvements over the older versions of QIE. QIE8 is produced in the AMS 0.8u BiCMOS process, a "true" BiCMOS process (previous QIE's were produced in the pseudo-BiCMOS 2u ORBIT process).

QIE is an acronym for the functions of the ASIC, Q (charge) I (integration) and E (encode). A large dynamic range is accomplished through a multi-range technique. The input current is simultaneously integrated on all ranges, and comparators are used to select the lowest range that is not at full scale. The selected voltage representing the integrated charge is then put through an on-chip Flash ADC (FADC). The outputs are a 5 bit mantissa representing the voltage and a two-bit code indicating the range. Operations are time multiplexed and pipelined to allow signals to settle and to make the reset interval the same as the integration interval. Clocking takes place at 40Mhz and the latency is 100ns as the pipeline is four clock cycles deep.

A top level block diagram of the QIE8 is shown in Figure 1. In Figures 2 and 3, the current amplifier/splitter designs for the non-inverting and inverting inputs are shown. As can be seen, the current splitter design uses outputs which are x5, x1, x1 and x1 for each of the four possible ranges. The range weighting is done in the phase block, shown in Figure 4, by ratioing the integrating capacitor value (/1, /1, /5, and /25) of the integrating amplifiers for each range. Thus; when taking these two scaling factors into account, the four ranges measure charge in increasing factors of 5 (x1, x5, x25, and x125).

There are four sets of charge integrating capacitors, or phase blocks, in QIE8. One set of capacitors integrates the input current for one beam crossing interval; the clock frequency is equal to the beam-beam collision frequency (40Mhz). While one set of capacitors is collecting charge, others are being read out and reset. At any given point in time, one set of charge integrating capacitors is collecting charge, one is settling, one is being read out, and one is being reset.

A DC bias current is added to the input current. One of the functions of the bias current is to provide a minimum current in the splitter to ensure that the transistors are in a good operating region.

For a given charge deposition over one clock interval, no more than one capacitor in the set will have its voltage within specified limits. The voltage on this capacitor is digitised by an on-board chip FADC. The FADC is piecewise linear. It is built with 15 bins weighted 1, 7 bins weighted 2, 4 bins weighted 3, 3 bins weighted 4 and 3 bins weighted 5. The priority encoded address of this capacitor makes up the exponent bits. The voltage on the capacitor is the mantissa and the address of the capacitor is the exponent.

QIE8 has two independent input amplifiers, one inverting and one non-inverting so that it can accept either polarity input signal. The non-inverting input is meant to accept a fast negative current PMT signal driven down a cable of significant length. It therefore has an impedance which is nearly constant over the entire range, in order to properly

terminate a cable. The input impedance is selectable between two values, 50 and 93 ohms. The amplifier gain is approximately one, resulting in a low end sensitivity of 2.6 fC/ bit. The maximum charge accepted per bucket is approximately 26 pC, yielding a 10,000:1 dynamic range, or at least 13 bits. The non-inverting amplifier has a fast response to allow complete integration of a fast PMT pulse in one 25 nS bucket.

The inverting amplifier is meant to accept positive current input pulses from HPD's. Since HPD signal levels are low, the amplifier has a current gain of –2.6, resulting in a low end sensitivity of 1 fC/bit. The maximum input charge per bucket is then approximately 10 pC. Since HPD pulses are slower (stretched over several buckets), the inverting amplifier response is slower than the non-inverting amplifier, in order to limit noise. Also, its input impedance is low (30 ohms or less) but not constant over the full range, since this input is intended to be driven with a relatively short cable.

The user must select which input amplifier will be used by powering only the one desired, and grounding the power pin of the amplifier which will not be used.

QIE8 also provides a calibration mode. When the CALMODE input signal is high, the QIE8 will use a strictly linear FADC. This results in a calibration scale of 32 linear counts output, which are weighted 0.87 fC/count in the non-inverting mode and 1/3 fC/count in the inverting mode.
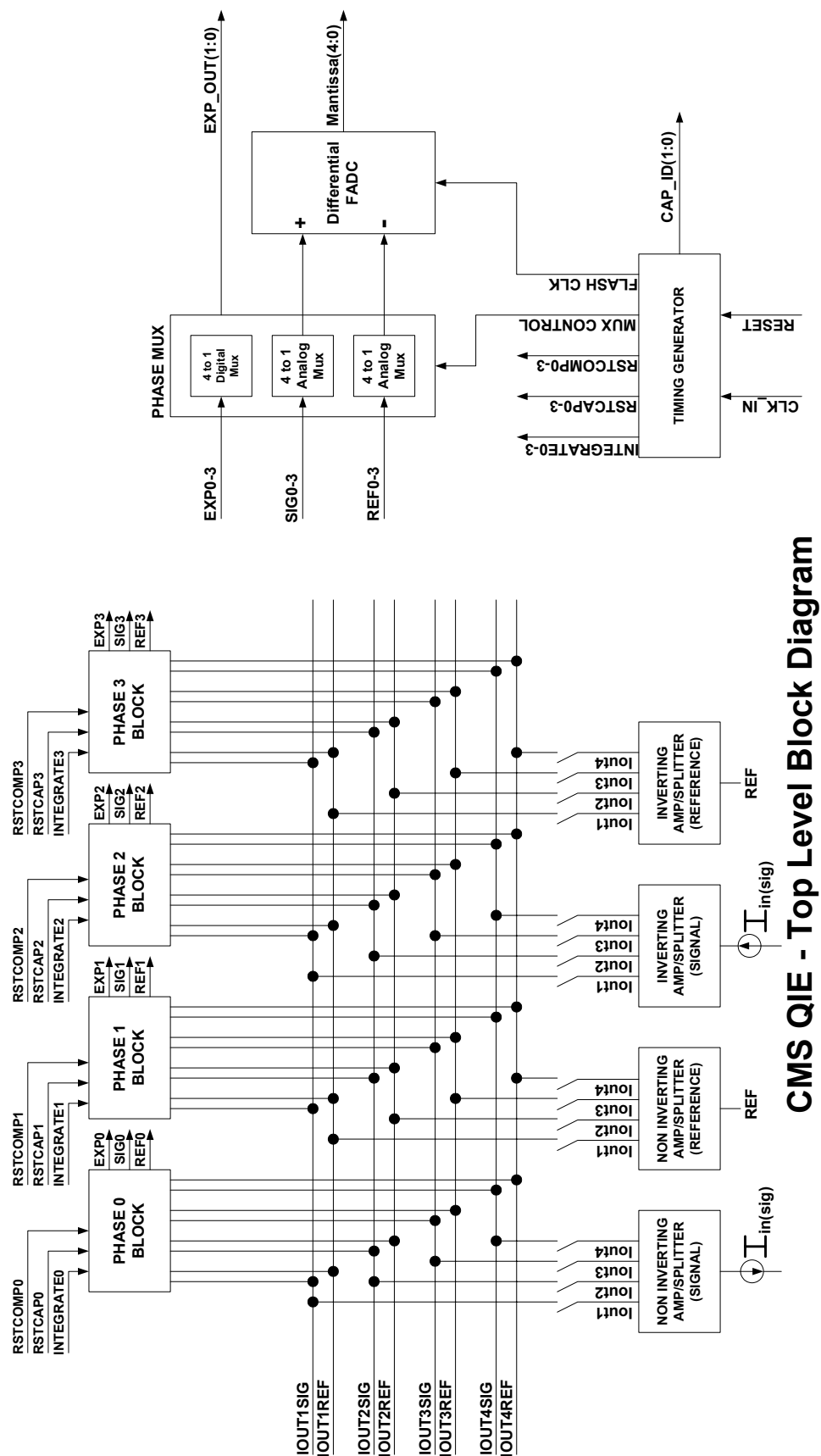
Figure 1. Top Level Block Diagram of QIE8

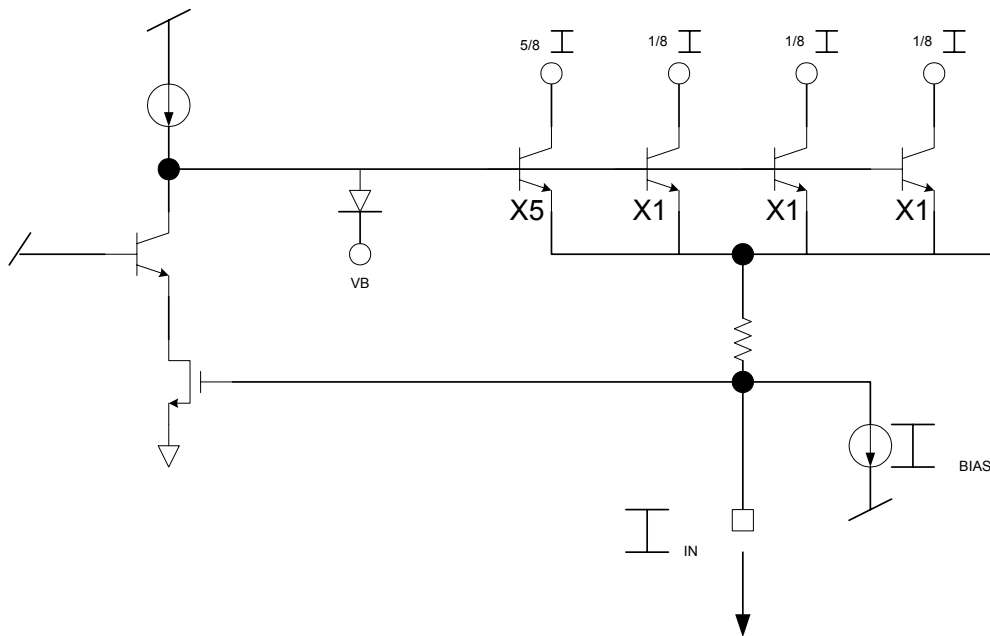**Figure 2. QIE8 Non-Inverting Amplifier/Splitter**

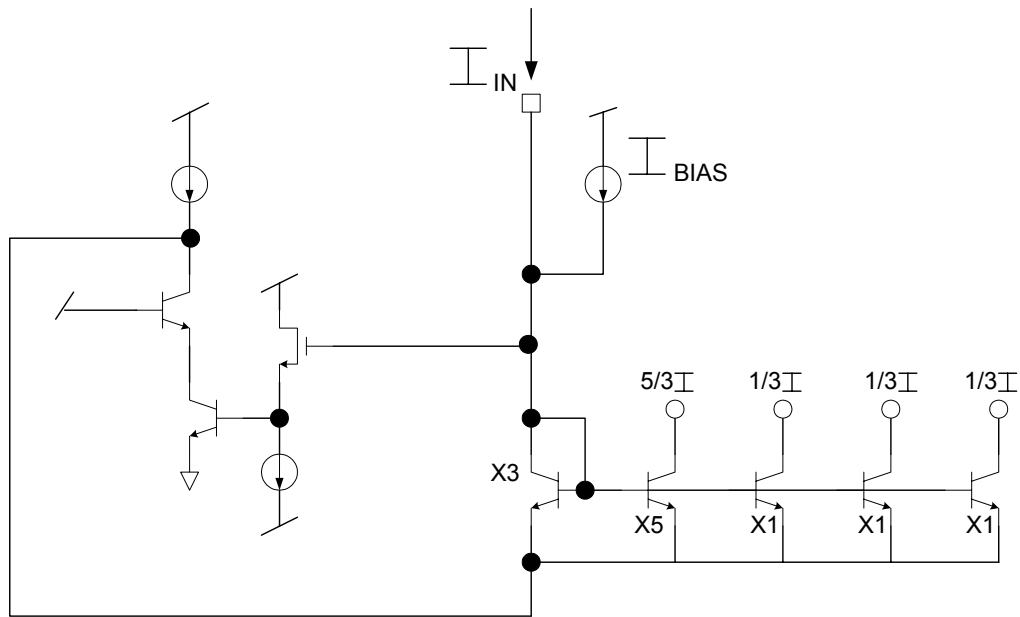**Figure 3. QIE8 Inverting Amplifier/Splitter**
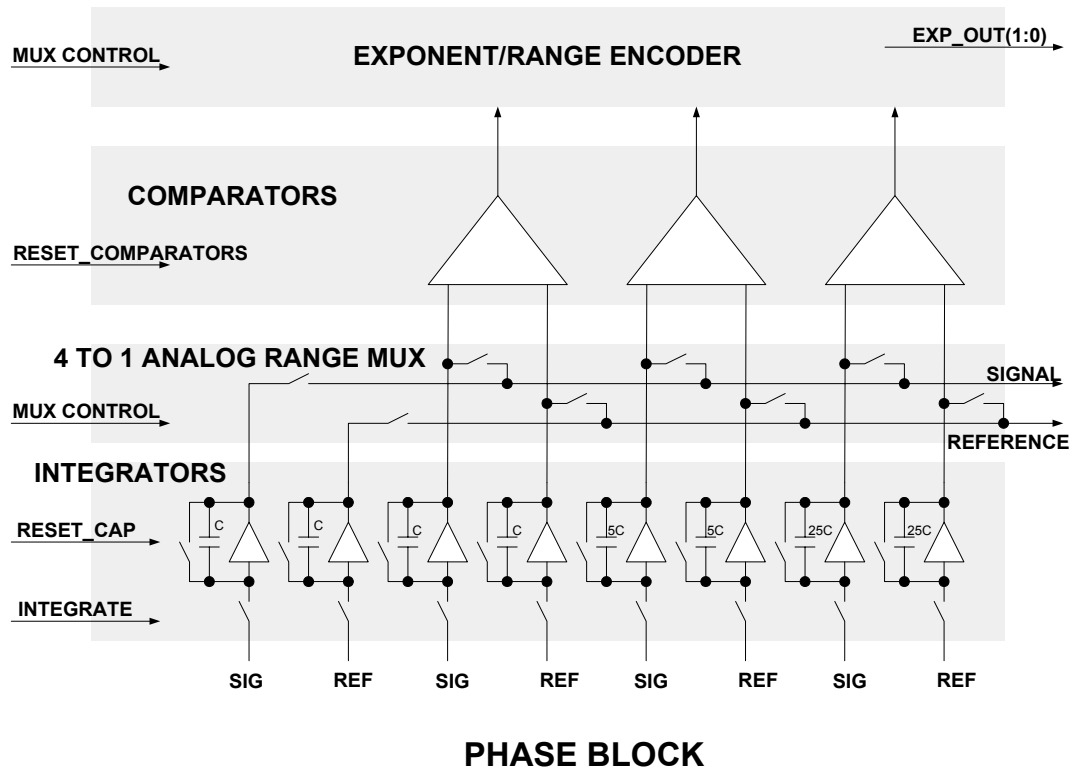
PHASE BLOCK

Figure 4. QIE8 Phase Block

Power:

Power Dissipation ~ 350mW
Supply Voltage:
        VDD/VCC: 5.0-5.5V
Package: 68 pin TQFP

Following is a table which maps out the nominal charge sensitivity of the QIE8 over its 4 ranges. **The actual sensitivity will depend on process variations, but should be within 20% of nominal.** Note that each range is piece-wise linear, with the ADC assuming a "pseudo-logarithmic" response. In this way, the 5-bit ADC covers a 6-bit range, and tends to have a more constant resolution. The sensitivity at the bottom of a range is 5 times that at the top. Since adjacent range sensitivities differ by a factor of 5, the sensitivity at the top of a given range is the same as at the bottom of the next range. The calibration mode, intended to be used at the bottom of Range 0 only, offers 3 times higher sensitivity with limited range and linear response only.

Inverting Input Scale (HPD Inputs)

Normal Mode			
Range (Exponent)	Input Charge	FADC Codes	Gain (q/Lsb)
0	-1 fC --- 14 fC	0---14	1 fC/bin
0	14 fC --- 28 fC	15---21	2 fC/bin
0	28 fC --- 40 fC	22---25	3 fC/bin
0	40 fC --- 52 fC	26---28	4 fC/bin
0	52 fC --- 67 fC	29---31	5 fC/bin
1	57 fC --- 132 fC	0---14	5 fC/bin
1	132 fC --- 202 fC	15---21	10 fC/bin
1	202 fC --- 262 fC	22---25	15 fC/bin
1	262 fC --- 322 fC	26---28	20 fC/bin
1	322 fC --- 397 fC	29---31	25 fC/bin
2	347 fC --- 722 fC	0---14	25 fC/bin
2	722 fC --- 1072 fC	15---21	50 fC/bin
2	1072 fC --- 1372 fC	22---25	75 fC/bin
2	1372 fC --- 1672 fC	26---28	100 fC/bin
2	1672 fC --- 2047 fC	29---31	125 fC/bin
3	1797 fC --- 3672 fC	0---14	125 fC/bin
3	3672 fC --- 5422 fC	15---21	250 fC/bin
3	5422 fC --- 6922 fC	22---25	375 fC/bin
3	6922 fC --- 8422 fC	26---28	500 fC/bin
3	8422 fC --- 10297 fC	29---31	625 fC/bin
Calibration Mode			
Forced 0	-2.333 fC ---- 10 fC	0---31	1/3 fC/Bin

Table 1. QIE Inverting Input Scale

Non-Inverting Input Scale (PMT inputs)

Normal Mode			
Range (Exponent)	Input Charge	FADC Codes	Gain (q/Lsb)
0	-3 fC --- 36 fC	0---14	2.6 fC/bin
0	36 fC --- 73 fC	15---21	5.2 fC/bin
0	73 fC --- 104 fC	22---25	7.8 fC/bin
0	104 fC --- 135 fC	26---28	10.4 fC/bin
0	135 fC --- 174 fC	29---31	13 fC/bin
1	150 fC --- 343 fC	0---14	13 fC/bin
1	343 fC --- 525 fC	15---21	26 fC/bin
1	525 fC --- 681 fC	22---25	39 fC/bin
1	681 fC --- 837 fC	26---28	52 fC/bin
1	837 fC --- 1032 fC	29---31	65 fC/bin
2	902 fC --- 1877 fC	0---14	65 fC/bin
2	1877 fC --- 2787 fC	15---21	130 fC/bin
2	2787 fC --- 3567 fC	22---25	195 fC/bin
2	3567 fC --- 4347 fC	26---28	260 fC/bin
2	4347 fC --- 5322 fC	29---31	325 fC/bin
3	4672 fC --- 9547 fC	0---14	325 fC/bin
3	9547 fC --- 14097 fC	15---21	650 fC/bin
3	14097 fC --- 17997 fC	22---25	975 fC/bin
3	17997 fC --- 21897 fC	26---28	1300 fC/bin
3	21897 fC --- 26772 fC	29---31	1625 fC/bin
Calibration Mode			
Forced 0	--6.1 fC ---- 26 fC	0---31	0.86 fC/Bin

Table 2. QIE Non-Inverting Input Scale

QIE8 Pinout

The QIE8 die has 64 pads which must be bonded. It is intended to be packaged in a 64 pin package, see Figure 5. However, the fact that the number of chip pads and package pins is identical is actually quite coincidental. This is due to the fact that the chip is bonded in a non-standard fashion – each bondpad does not necessarily go to a package pin. The metal die pad inside the package serves as "system ground," and all of the chip ground pads are bonded directly down to the die pad inside the package. The die pad is then bonded out to a number of package ground pins in various locations.

The following pin naming conventions are observed: Inputs and control pins which are associated with the non-inverting input are prefaced with **NI_**. Inputs and control pins which are associated with the inverting input are prefaced with **I_**. Every input pin is surrounded on both sides by ground pins. Each input that is routed to the QIE8 on a PC board must be routed on an inner layer and fully enclosed by ground planes and traces. The ground planes should come at least up to the input side of the package, where they must connect directly to all 8 ground pins on that side of the package. No other "analog ground plane" is needed on the PC board. Supporting digital circuitry on the PC board should be placed nearest the QIE8 output edge, completely away from the input edge. There should be a "digital ground plane" for all digital circuitry on the PC board. This plane should extend under the QIE8 digital output traces (but should not extend under the QIE8) and be connected to the QIE8 ground at ONE place only, the DGND1,2 pins.

Analog and digital power pins (**AVDD** and **DVDD**) can be driven by a single supply regulator (5.0V min., 5.5V max.). However, the pins should not be tied to a "power plane." Separate traces which are tied together close to the 5V regulator should supply these pins. The supply regulator ground should connect to the PC board digital ground plane.

The non-inverting and inverting input amplifier sections each have their own analog supply pins (**NI_AVDD** and **I_AVDD**). Only one amplifier is intended to be used at a time (although theoretically both could be used simultaneously). The unused amplifier should have its AVDD pin tied to ground.

The **AGND** pins on the left edge do not necessarily need to be connected to "ground plane." They are provided to offer easy routing of **AVDD** and **NI_CLAMP** bypass capacitors (**AGND** pins connect the caps to the internal die pad ground). A digital supply bypass capacitor is required, but must NOT be placed to any ground plane. It should simply be connected from the **DVDD** pins to the **DGBYP** pin.
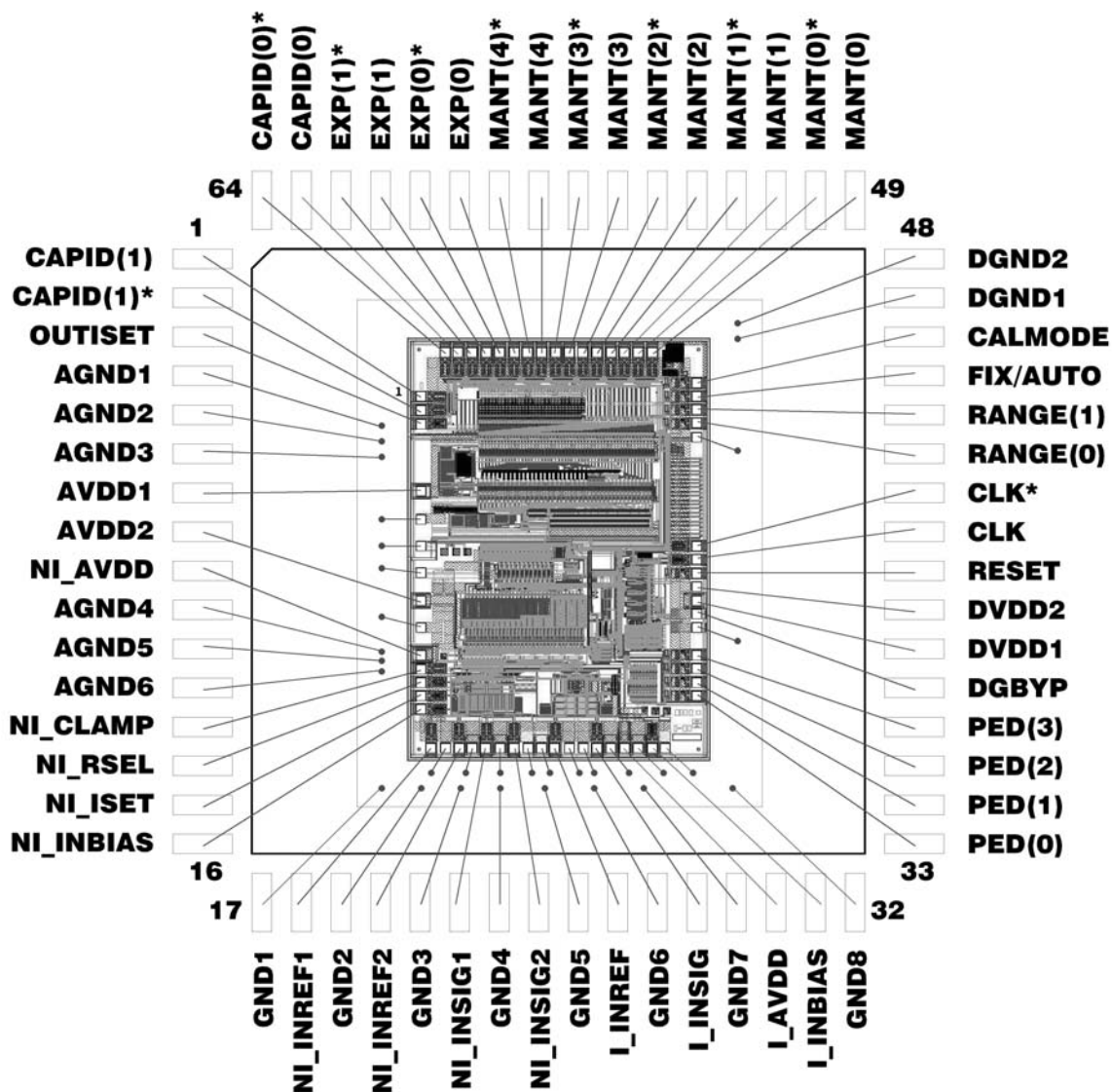
Figures 6 and 7 are simple representations of the PCB routing which we have found effective.

07/18/02

QIE 8 Production Pinout
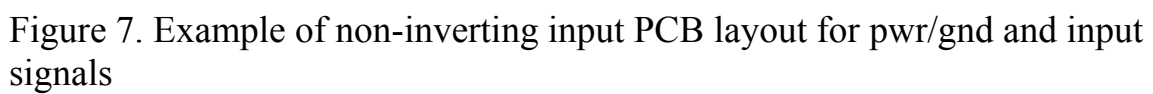## 64-Lead TQFP Package Bonding Diagram
(Drawing NOT to Scale)

QIE 8 Die Size: 3.070mm x 4.350mm
Die bond pad opening: 85 micron x 85 micron
Die bond pad pitch: 140 micron
Die bond pad metalization: Al (1%Si, 1%Cu)
Die Attach: Thermally Conductive

Notes: Package Pins 4, 5, 6, 10, 11, 12, 17, 19, 21, 23, 25, 27, 29, 32, and 47, 48 are bonded to the die attach pad.

Figure 5. QIE8 Packaging and Pinout

Figure 6. Example of inverting input PCB layout for pwr/gnd and input signals.

Figure 7. Example of non-inverting input PCB layout for pwr/gnd and input signals

CMS QIE (QIE8) Production Pinout

Pin #	Pin Name		Pin #	Pin Name
1	CAPID(1)		33	PED(0)
2	CAPID(1)*		34	PED(1)
3	OUTISET		35	PED(2)
4	AGND1		36	PED(3)
5	AGND2		37	DGBYP
6	AGND3		38	DVDD1
7	AVDD1		39	DVDD2
8	AVDD2		40	RESET
9	NI_AVDD		41	CLK
10	AGND4		42	CLK*
11	AGND5		43	RANGE(0)
12	AGND6		44	RANGE(1)
13	NI_CLAMP		45	FIX/AUTO
14	NI_RSEL		46	CALMODE
15	NI_ISET		47	DGND1
16	NI_INBIAS		48	DGND2
17	GND1		49	MANT(0)
18	NI_INREF1		50	MANT(0)*
19	GND2		51	MANT(1)
20	NI_INREF2		52	MANT(1)*
21	GND3		53	MANT(2)
22	NI_INSIG1		54	MANT(2)*
23	GND4		55	MANT(3)
24	NI_INSIG2		56	MANT(3)*
25	GND5		57	MANT(4)
26	I_INREF		58	MANT(4)*
27	GND6		59	EXP(0)
28	I_INSIG		60	EXP(0)*
29	GND7		61	EXP(1)
30	I_AVDD		62	EXP(1)*
31	I_INBIAS		63	CAPID(0)
32	GND8		64	CAPID(0)*

Table 3. CMS QIE (QIE8) Production Pinout

Signal Definitions

CAPID(1:0)

CapID(1) output MSB. (CapID is a 2 bit number representing which of the four pipelined integrating capacitors is being read out). The Cap ID outputs are read out as a low level differential voltage signal with LVDS-like levels, but with internal terminations (approx. 400 ohms). These outputs are only intended to drive a short distance (approx. 10 pF load) and are not intended to be terminated externally.

CAPID(1:0)*

Cap ID output MSB complement.

OUTISET

This pad gives external access to the bias circuit for the low level differential voltage output drivers (CapIDs, EXPONENTs, and MANTISSAs). It is included mostly for test purposes and nominally should be left unconnected. A resistor can be connected from VDD to this pad to increase the output drive level. The nominal resistance which exists internally is 3.4K.

AGND1 – AGND3

Analog ground pins, any or all of which can be used to return the bypass capacitor (for **AVDD1**, **AVDD2**, and **NI_AVDD**) to the internal die pad (analog ground).

AVDD1 – AVDD2

Analog power supply pins. Connect together to +5V supply. Bypass to one or all of **AGND1,2,3**.

NI_AVDD

Non-inverting input amplifier power supply pin. Connect to +5V together with **AVDD1,2** if using the non-inverting input. Otherwise, connect to ground (**AGND4** is closest and easiest) to disable.

AGND4 – AGND6

Analog ground pins, any or all of which can be used to return the **NI_CLAMP** bypass capacitor to the internal die pad (analog ground).

NI_CLAMP

Non-inverting input amplifier bias voltage, which must be bypassed to ground with an external capacitor of 0.1 uF. The bypass cap can be connected to any or all of **AGND4,5,6** to return it to the internal die pad analog ground. The **NI_CLAMP** voltage is generated internally, but can be externally pulled in order to tweak the input impedance value if necessary. Place an external resistor to ground or VDD as required.

NI_RSEL

Selects the input impedance of the non-inverting input amplifier. If unconnected, this pad defaults high (VDD), which sets the input impedance to 93 ohms. If grounded, the input impedance is 50 ohms.

NI_ISET

Non-inverting amplifier bias. Since the input impedance of the non-inverting amplifier is dependent on this bias value, no internal bias set resistor is present. A 1% tolerance external resistance should be used to set this bias value. Nominal is a 14K resistor to ground (300 uA).

NI_INBIAS

Non-inverting amplifier DC input bias current set. Set by connecting a resistor from this pad to VDD. The internal bias current will actually be 4 times smaller than the set value. Nominal set current is approximately 16 uA (4 uA amplifier bias), which gives enough bandwidth to integrate a fast PMT pulse in one 25 ns bucket. This bias current can be adjusted to tailor the bandwidth. For nominal bias, use 220K.

GND1 – GND8

> Input signal ground pins. The ground planes which encase the signal traces should be connected directly to all of these pins.

NI_INREF1

> Non-inverting amplifier reference input #1. This reference input ideally will have a cable or interconnect attached to it which looks identical to the signal input (although the reference input should actually have no signal applied to it).

NI_INREF2

> Non-inverting amplifier reference input #2. An external resistor must be connected between reference input #1 and reference input #2. The value of this resistor depends on the desired input impedance. For 50 ohm input impedance, the R value should be 56 ohms, and for 93 ohm input impedance it should be 110 ohms.

NI_INSIG1

> Non-inverting amplifier signal input #1. The signal input trace should be connected directly to this input, and should be completely encased with ground planes and traces right up to the pin.

NI_INSIG2

> Non-inverting amplifier signal input #2. An external resistor must be connected between signal input #1 and signal input #2. The value of this resistor depends on the desired input impedance. For 50 ohm input impedance, the R value should be 56 ohms, and for 93 ohm input impedance it should be 110 ohms.

I_INREF

> Inverting amplifier reference input. This reference input ideally will have an interconnect attached to it which looks identical to the signal input (although the reference input should actually have no signal applied to it).

I_INSIG

> Inverting amplifier signal input. The input trace should be completely encased with ground planes and traces right up to the pin.

I_AVDD

> Inverting input amplifier power supply pin. Connect to +5V (tie to **AVDD1,2)** if using the inverting input. Bypass with 0.1 uF from the pin to the ground plane which is connected to **GND1-8**. If the inverting input is not used, connect **I_AVDD** to ground.

I_INBIAS

> Inverting amplifier DC input bias current set. Set by connecting a resistor from this pad to ground. The internal bias current will actually be 4 times smaller than the set value. Nominal set current is approximately 4 uA (1 uA amplifier bias), giving a bandwidth appropriate for an input pulse which spans about 3 buckets (75 ns). The bias current can be adjusted to tailor the bandwidth. For nominal bias, use 750K.

PED(3:0)

> Pedestal DAC inputs. Bits 0-2 control the pedestal magnitude (binary code, bit 0 is LSB) and bit 3 controls the polarity. Bit 3 low gives positive pedestals, and high gives negative pedestals. Each DAC bit gives approx. 0.6 ADC bits of pedestal, therefore the pedestal range is from 0 to about 4 ADC bits, in each direction. If unconnected, the DAC pads all default low.

DGBYP

> Digital ground bypass. This pin is for returning the DVDD bypass cap to internal die pad ground. It should NOT be externally grounded.

DVDD1 – DVDD2

Digital supply connections (the two pins are redundant, only one is necessary). Connect to the same +5V supply as AVDD, but with a separate trace. Bypass locally as tightly as possible with a 0.1 uF capacitor from **DVDD** to **DGBYP**.

RESET

QIE reset signal. The reset signal should be approximately one clock period in duration. Each edge should occur near a positive going edge of the CLK signal. RESET is designed to accept a 3.3V CMOS level. A 5V CMOS level is also acceptable. After application of the reset, the capID is set to 0.

CLK

Clock input signal. CLK – CLKB accepts a low level differential signal (LVDS levels). QIE8 is designed for 40 MHz operation.

CLK*

Clock input complement.

RANGE(1:0)

Range 0,1 form a binary code which determines the range when the QIE8 is in fixed range mode (**FIX/AUTO** pin high). When in autorange mode (**FIX/AUTO** low), these bits have no effect, and the QIE8 automatically determines the appropriate range. Input levels are 3.3V CMOS. If unconnected, they default low.

FIX/AUTO

Selects between fixed range mode (range determined by range 0,1 bits) and autorange mode. 3.3V CMOS level. Low selects autorange, high selects fixed range. If unconnected, defaults low.

CALMODE

Selects between normal mode and calibration mode. 3.3V CMOS level. Low selects normal mode, high selects calibration mode. Calibration is a high sensitivity (3X) limited span mode intended to be used only on the low range of the QIE8. (See table below). It allows a gain calibration to be performed by an input current source which has a magnitude of less than 1 LSB. If unconnected, **CALMODE** defaults low.

DGND1 – DGND2

Pins to the internal die pad ground which should be connected to the PC board digital ground plane. This should be the only connection point between the PCB digital ground and the QIE8 ground. The pins are redundant.

MANT(4:0)

Five bit mantissa (ADC) output bit. All outputs are low level differential voltage, as explained for the CapID bit.

MANT(4:0)*

Complement of MANT(4:0).

EXP(1:0)

Two bits of exponent (range) output.

EXP(1:0)*

Complement of EXP(1:0).

QIE Timing Requirements for RESET

The QIE_RESET signal is used to reset the internal state machine which controls the selection of the four capacitor banks. A QIE_RESET allows the user to re-synchronize the system.

Figure 8 shows that the CapID resets to "Y" and that the next rising edge of QIE_CLK advances the CapID to "YY". (Note Y and YY TBD)
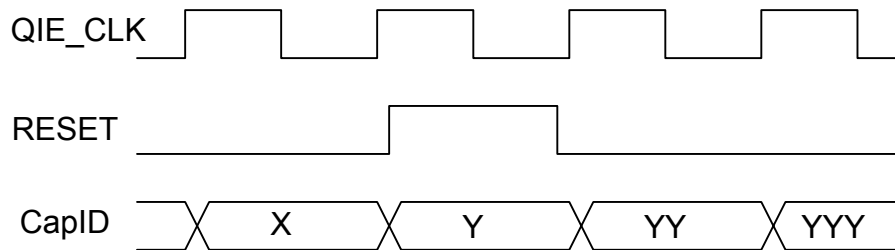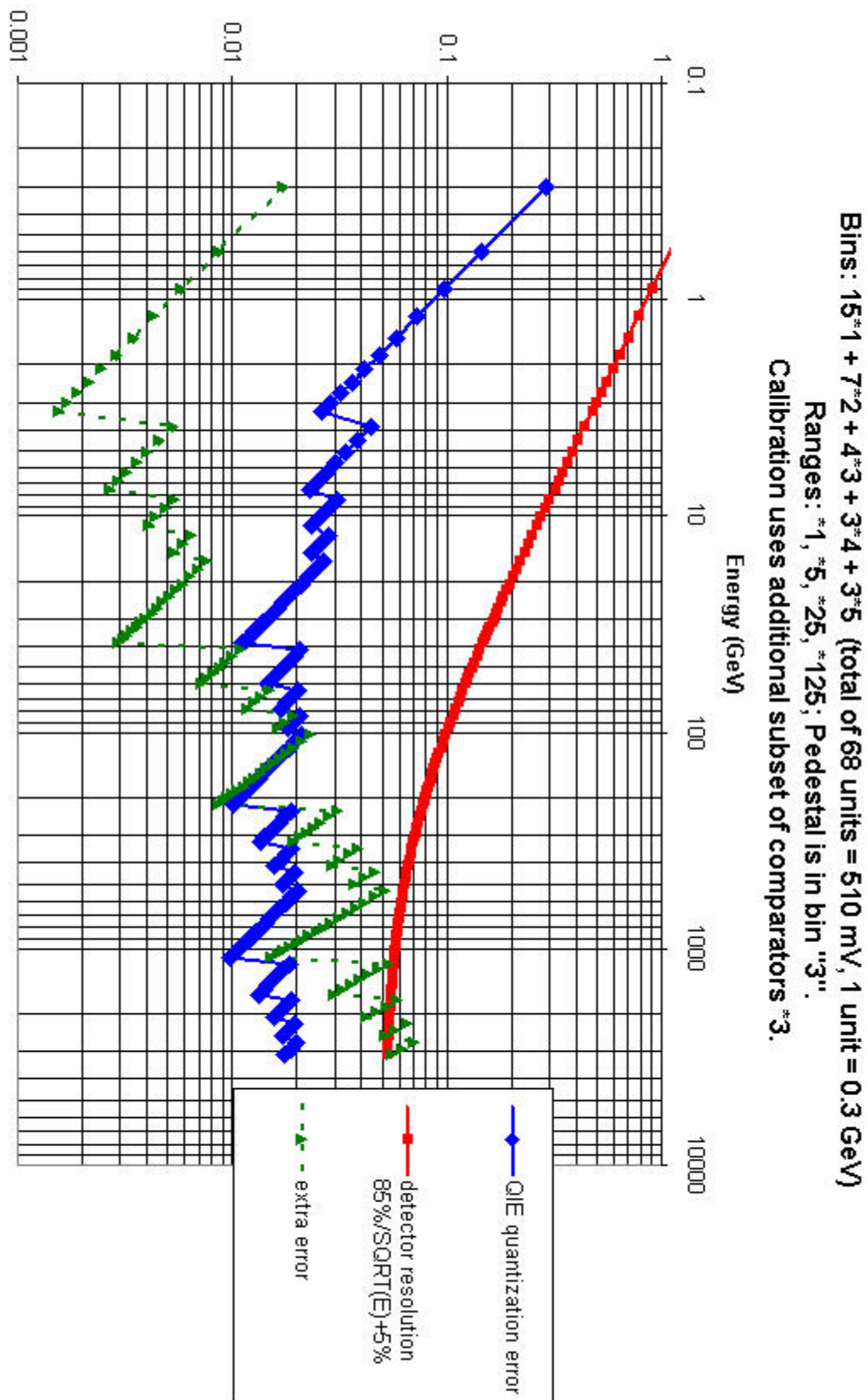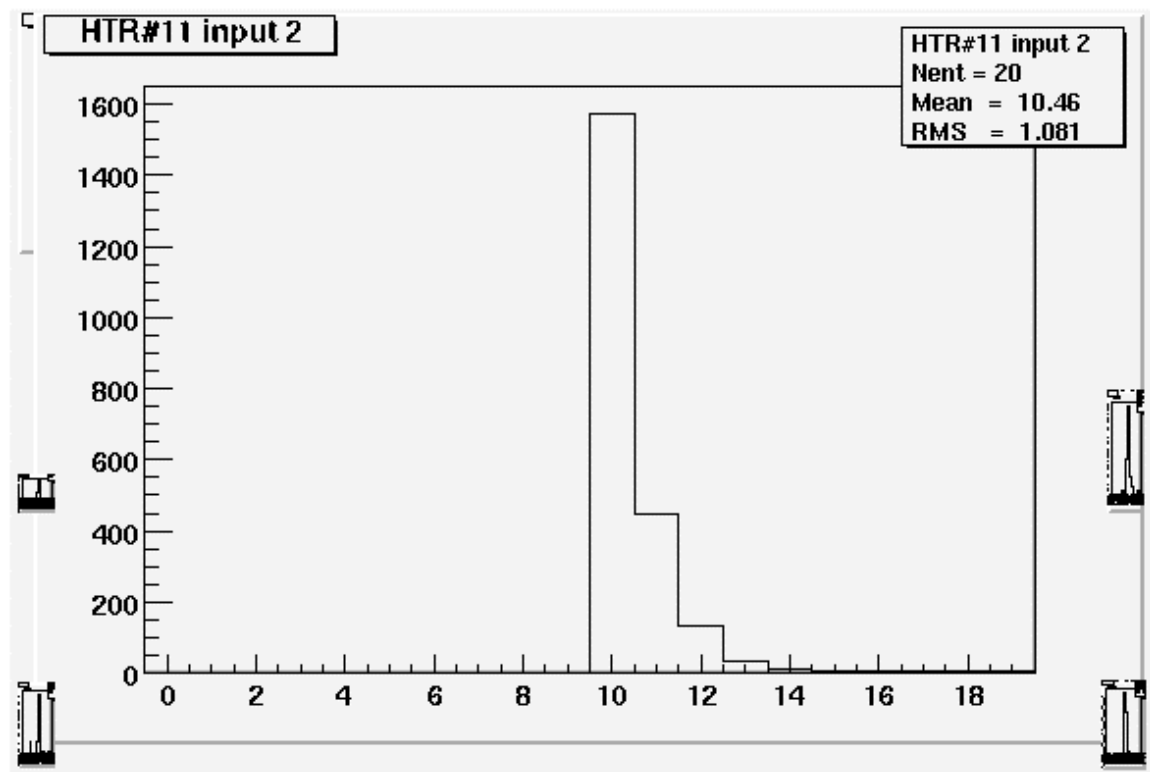

Figure 8. Reset Timing

Appendix A

Flash ADC Quantization Effects

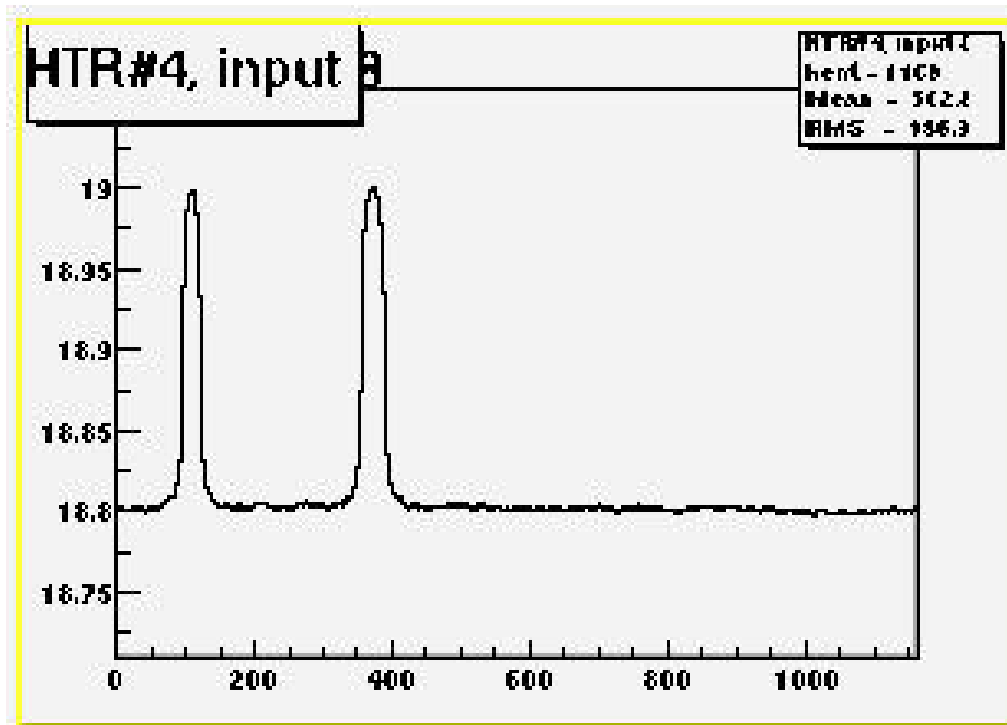**QIE Flash ADC Quantization Graph**

Appendix B

Some QIE Results as Readout through CMS FE Electronics

300 Gev Pion at seen at 2002 Testbeam

Source Run at 2002 Testbeam (Source seen moving in and out)

A Pipelined Multiranging Integrator and Encoder ASIC for Fast Digitization of Photomultiplier Tube Signals, R. Yarema et al, Fermilab-Conf-92/148.

A Second Generation Charge Integrator and Encoder ASIC, T. Zimmerman and M. Sarraj, IEEE NS V43#3, June 1996.